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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/684,224	10/10/2003	Chen-Hua Yu	TSM03-0403	8634

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SLATER & MATSIL, L.L.P.
17950 PRESTON ROAD, SUITE 1000
DALLAS, TX 75252

EXAMINER
WILLIAMS, ALEXANDER O

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

H'A

Office Action Summary	**Application No.** 10/684,224	**Applicant(s)** YU ET AL.	
	Examiner Alexander O. Williams	**Art Unit** 2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 July 2005*.
2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.
3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.
  4a) Of the above claim(s) *32-56* is/are withdrawn from consideration.
5)☐ Claim(s) _____ is/are allowed.
6)☒ Claim(s) *1-31* is/are rejected.
7)☐ Claim(s) _____ is/are objected to.
8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.
10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.
  Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
  Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
  a)☐ All b)☐ Some * c)☐ None of:
    1.☐ Certified copies of the priority documents have been received.
    2.☐ Certified copies of the priority documents have been received in Application No. _____.
    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
  * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
  Paper No(s)/Mail Date *2/2/04*.
4) ☐ Interview Summary (PTO-413)
  Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/684224 Attorney's Docket #: TSM03-0403
Filing Date: 10/10/2003;

Applicant: Yu et al.

Examiner: Alexander Williams

Applicant's election of Group I (claims 1 to 31), filed 7/12/05, has been acknowledged.

This application contains claims 32 to 56 drawn to an invention non-elected without traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 3, 6 to 16, 19 to 21 and 24 to 31 are rejected under 35 U.S.C. § 102(e) as being anticipated by Hartner et al. (U.S. Patent # 6,649,483 B2).

1. Hartner et al. (figures 1 to 3D) specifically figure 2 show a semiconductor device comprising: a dielectric layer **30** defining at least one aperture therein; a barrier layer **12** formed along the bottom and side walls of said at least one aperture; a high temperature superconductor (HTS) layer **(within 10)** formed over the barrier layer in said at least one aperture; and a conductive material filling **(within 10)** said aperture in said dielectric layer.

3. The semiconductor device of claim 1, Hartner et al. show wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations of these materials.

6. The semiconductor device of claim 1, Hartner et al. show wherein the HTS material is a rare earth cuprate (copper oxide) material.

7. The semiconductor device of claim 1, Hartner et al. show wherein the HTS material is a rare earth element combined with barium copper oxide.

8. The semiconductor device of claim 7, Hartner et al. show wherein said rare earth element is selected from the group consisting of **yttrium**, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holnuum and lutetium.

9. The semiconductor device of claim 7, Hartner et al. show wherein the HTS material is yttrium barium copper oxide.

10. The semiconductor device of claim 1, Hartner et al. show wherein said HTS layer is a rare earth Ruthenium Oxocuprate.

11. The semiconductor device of claim 10, Hartner et al. show wherein said rare earth Ruthenium Oxocuprate is defined by the formula RuSr, (rare earth element) CuyOZ in which x is between about 1.55 and 2.45, y is between about 1.55 and 2.45, and z is between about 7.55 and 8.45.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

12. The semiconductor device of claim 11, Hartner et al. show wherein said rare earth element is selected from the group consisting of **yttrium**, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.
13. The semiconductor device of claim 1 wherein the FITS layer has a thickness of between 10A to 500A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

14. The semiconductor device of claim 1, Hartner et al. show wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.
15. The semiconductor device of claim 1 wherein the aperture defined in said dielectric has a width less than about 300.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The semiconductor device of claim 3, Hartner et al. show wherein the aperture defined in said dielectric has a width less than about 300.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

19. The semiconductor device of claim 1, Hartner et al. further comprising a capping layer over said conductive metal filling said at least one aperture.
20. The semiconductor device of claim 19, Hartner et al. show wherein said capping layer is an HTS capping layer.
21. The semiconductor device of claim 19, Hartner et al. further comprising another dielectric layer over said first dielectric layer and said HTS capping layer.
22. The semiconductor device of claim 19, Hartner et al. further including a hard mask over said HTS

capping layer.
24. The semiconductor device of claim 21 wherein said HTS capping layer has a thickness between about 10 A and 500 A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

25. Hartner et al. (figures 1 to 3D) specifically figure 2 show a semiconductor device comprising:
a first dielectric layer **30** defining at least one aperture therein;
a conductive material filling **(within 10)** said at least one aperture in said first dielectric layer;
an HTS capping layer **(within 10)** over said conductive material filling said at least one aperture; and another dielectric layer **40** over said first dielectric layer and said HTS capping layer.
26. The semiconductor device of claim 25, Hartner et al. show wherein said HTS capping layer has a thickness of 2 between about 10 A and 500 A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

27. The semiconductor device of claim 25, Hartner et al. show wherein said aperture in said first dielectric layer has a width less than about 300 A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

28. The semiconductor device of claim 25, Hartner et al. show wherein the HTS material is a rare earth cuprate (copper oxide) material.
29. The semiconductor device of claim 25, Hartner et al. show wherein the HTS material is a rare earth element combined with barium copper oxide.
30. The semiconductor device of claim 29, Hartner et al show wherein said rare earth element is selected from the group consisting of **yttrium**, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.
31. The semiconductor device of claim 29, Hartner et al. show wherein the HTS material is yttrium barium copper oxide.

US-PAT-NO: 6649483

DOCUMENT-IDENTIFIER: US 6649483 B2

TITLE: Method for fabricating a capacitor configuration

DATE-ISSUED: November 18, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hartner; Walter	Glen Allen	VA	N/A	N/A
Weinrich; Volker	Paris	N/A	N/A	FR
Kronke; Matthias	Dresden	N/A	N/A	DE

ASSIGNEE INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Infineon Technologies AG	Munich	N/A	N/A	DE	03

APPL-NO: 09/ 996959

DATE FILED: November 20, 2001

1. (36) In order to fabricate ferroelectric capacitors for applications in nonvolatile semiconductor memories having a high integration density, a ferroelectric material, for example SrBi.sub.2 (Ta,Nb).sub.2 O.sub.9 (SBT, SBTN), Pb(Zr,Ti)O.sub.3 (PZT), Bi.sub.4 Ti.sub.3 O.sub.12 (BTO), (Ba,Sr)TiO.sub.3 (BST) or the like, is used as a dielectric between the electrodes of a capacitor. **Paraelectric materials, such as, for example,**
2. **(Ba,Sr)TiO.sub.3 (BST), can also be used. The electrode material is a noble metal which withstands high temperatures in oxygen. Appropriate materials for this are Pt, Pd, Ir, Rh, Ru, RuO.sub.x, IrO.sub.x, RhO.sub.x, SrRuO.sub.3, LSCO (LaSrCoO.sub.x), YBa.sub.2 Cu.sub.3 O.sub.7** and high-temperature superconductors. In general, the capacitor construction involves, in a conventional manner, either following the technologically more demanding stacked principle or else

> proceeding according to the offset cell principle, which takes up a great deal more space.

Claims 1, 2, 3, 6 to 9 and 13 to 31 are rejected under 35 U.S.C. § 102(e) as being anticipated by Lopatin (U.S. Patent # 6,518,648 B1).

1. Lopatin (figures 1 to 3) specifically figure 3 show a semiconductor device comprising: a dielectric layer **208** defining at least one aperture therein; a barrier layer **226** formed along the bottom and side walls of said at least one aperture; a high temperature superconductor (HTS) layer **226,232** formed over the barrier layer in said at least one aperture; and a conductive material filling **236** said aperture in said dielectric layer.

2. The semiconductor device of claim 1, Lopatin show wherein the dielectric layer is a low-k dielectric material.

3. The semiconductor device of claim 1, Lopatin show wherein the barrier layer is a material selected from a group consisting of titanium, titanium nitride, tantalum, tantulum nitride, tungsten, tungsten nitride, and alloys and combinations of these materials.

6. The semiconductor device of claim 1, Lopatin show wherein the HTS material is a rare earth cuprate (copper oxide) material.

7. The semiconductor device of claim 1, Lopatin show wherein the HTS material is a rare earth element combined with barium copper oxide.

8. The semiconductor device of claim 7, Lopatin show wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holnuum and lutetium.

9. The semiconductor device of claim 7, Lopatin show wherein the FITS material is yttrium barium copper oxide.

13. The semiconductor device of claim 1, Lopatin show wherein the HTS layer has a thickness of between 10A to 500A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

14. The semiconductor device of claim 1, Lopatin show wherein the conductive material is comprised of a material selected from a group consisting of copper, copper alloy, gold, silver, and compounds and combinations thereof.

15. The semiconductor device of claim 1, Lopatin show wherein the aperture defined in said dielectric has a width less than about 300.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

16. The semiconductor device of claim 3, Lopatin show wherein the aperture defined in said dielectric has a width less than about 300.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

17. The semiconductor device of claim 1, Lopatin show wherein said at least one aperture includes at least two trenches.

18. The semiconductor device of claim 17, Lopatin show wherein one of said at least two trenches further includes a via.

19. The semiconductor device of claim 1, Lopatin further comprising a capping layer over said conductive metal filling said at least one aperture.

20. The semiconductor device of claim19, Lopatin show wherein said capping layer is an HTS capping layer.

21. The semiconductor device of claim 19 further comprising another dielectric layer over said first dielectric layer and said HTS capping layer.

22. The semiconductor device of claim 19 further including a hard mask over said HTS capping layer.

24. The semiconductor device of claim 21 wherein said HTS capping layer has a thickness between about 10 A and 500 A,.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

25. Lopatin (figures 1 to 3) specifically figure 3 show a semiconductor device comprising:
a first dielectric layer **208** defining at least one aperture therein;
a conductive material filling **236** said at least one aperture in said first dielectric layer;
an HTS capping layer **226** over said conductive material filling said at least one aperture; and another dielectric layer over said first dielectric layer and said HTS capping layer **232**.

26. The semiconductor device of claim 25, Lopatin show wherein said HTS capping layer has a thickness of 2 between about 10 A and 500 A.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

27. The semiconductor device of claim 25, Lopatin show wherein said aperture in said first dielectric layer has a width less than about 300 A

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in

a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).
28. The semiconductor device of claim 25, Lopatin show wherein the HTS material is a rare earth cuprate (copper oxide) material.
29. The semiconductor device of claim 25, Lopatin show wherein the HTS material is a rare earth element combined with barium copper oxide.
30. The semiconductor device of claim 29, Lopatin show wherein said rare earth element is selected from the group consisting of yttrium, samarium, neodymium, erbium, gadolinium, ytterbium, dysprosium, holmium and lutetium.
31. The semiconductor device of claim 29, Lopatin show wherein the HTS material is yttrium barium copper oxide.

S-PAT-NO: 6518648

DOCUMENT-IDENTIFIER: US 6518648 B1
See image for Certificate of Correction

TITLE: Superconductor barrier layer for
integrated circuit
interconnects

DATE-ISSUED: February 11, 2003

INVENTOR-INFORMATION:
NAME CITY STATE
ZIP CODE COUNTRY
Lopatin; Sergey D. Santa Clara CA
N/A N/A

ASSIGNEE INFORMATION:
NAME CITY STATE ZIP
CODE COUNTRY TYPE CODE
Advanced Micro Devices, Sunnyvale CA N/A
N/A 02
Inc.

APPL-NO: 09/ 671944

DATE FILED: September 27, 2000

ABSTRACT:

An integrated circuit and manufacturing method therefor is provided having a semiconductor substrate with a semiconductor device. A dielectric layer is on the semiconductor substrate and has an opening provided therein. A high temperature superconductor material barrier layer lines the opening and a seed layer is deposited to line the superconductor material barrier layer. A seed layer and a conductor core fills the opening over the barrier layer to form a conductor channel. The superconductor material barrier layer can be of yttrium barium copper oxide deposited by a process, such as laser ablation (LA), chemical vapor deposition (CVD), atomic layer deposition (ALD), or self-ionized plasma (SIP) deposition on a low dielectric constant dielectric layer and having a copper seed layer deposited thereon by SIP deposition.

(11) The barrier layers 226 and 232 are of high temperature oxide superconductor materials such as yttrium barium copper oxide. The materials are multi-layered ceramics and are considered "high temperature" because at temperatures of 77.degree.-92.degree. Kelvin they are superconductive.

(12) The low dielectric constant dielectric layers 208, 212, and 210 are of materials such as TEOS (tetraethoxysilane), TMOS (tetramethoxysilane), OMCTS (octamethyleclotetrasiloxane), and DADBS (diaceloxyditerliarybutoxsilane). These materials are carried in a solvent fluid carrier such as MIBK (methyl isobutyl ketone). One of the more commonly used silicon-based, low dielectric constant materials is HSQ (hydrogen silsesquioxane) in MIBK solvent. A low dielectric constant material has a dielectric constant below 2.8 and is used to reduce capacitance effects which slow the operation of integrated circuits. Other low dielectric constant materials can be used.

(13) The seed layers 228 and 234 and conductor cores 230 and 236 are of materials such as copper, copper-base alloys, gold, gold-base alloys, silver, silver-base alloys, and a combination thereof.

(14) The method for manufacturing an integrated circuit having superconductor material barrier layers includes depositing the dielectric layer 208 over the semiconductor substrate by spin deposition.

(15) After processing the dielectric layer 208 to harden it, a photolithographic process is used to form an opening in the dielectric layer 208. An ammonia (NH.sub.3) plasma treatment is

used to treat the low dielectric constant dielectric material in preparation for the deposition of the superconductor material barrier layer 226 to line the opening.

(16) The superconductor material barrier layer 226 is deposited as a conformal barrier-liner by such processes as laser ablation (LA), chemical vapor deposition (CVD), atomic layer deposition (ALD), or self-ionized plasma (SIP) deposition. In the best mode for sub-0.18 .mu.m geometry copper interconnects, the superconductor material barrier layer 226 is deposited to a thickness of from 50 .ANG. to 300 .ANG..

Claims 4 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Lopatin (U.S. Patent # 6,518,648 B1) in view of Wo (U.S. Patent # 6,667,231 B1).

Lopatin show the features of the claimed invention as detailed above, but fail to explicitly show a layer of tantalum layer over the HTS layer or wherein the barrier layer comprises a layer of a tantalum-rich nitride over the HTS layer, and further comprising a layer of tantalum.

Wu et al. is cited for showing barrier films for copper metallizations over low dielectric contant insulators in a integrated circuit. Specifically, Wu (figures 1a to 2i) specifically figure 1a discloses a layer of tantalum layer (see column 3, lines 25-37) or wherein the barrier layer comprises a layer of a tantalum-rich nitride for the excellent adhesion.

US-PAT-NO:	6667231
DOCUMENT-IDENTIFIER:	US 6667231 B1
TITLE:	Method of forming barrier films for copper metallization over low dielectric constant insulators in an integrated circuit
DATE-ISSUED:	December 23, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wu; Lixin	Plano	TX	N/A	N/A

ASSIGNEE INFORMATION:
NAME CITY STATE ZIP
CODE COUNTRY TYPE CODE
Texas Instruments Dallas TX N/A
N/A 02
Incorporated

APPL-NO: 10/ 195006

DATE FILED: July 12, 2002

INT-CL: [07] H01L021/476

US-CL-ISSUED: 438/628, 438/622 , 438/677 , 438/679

US-CL-CURRENT: 438/628, 438/622 , 438/677 , 438/679

FIELD-OF-SEARCH: 438/622; 438/623 ; 438/624 ; 438/625 ; 438/626 ; 438/627 ; 438/628 ; 438/629 ; 438/688 ; 438/687 ; 438/677 ; 438/679

ABSTRACT:

An integrated circuit structure and method of making the same is disclosed, in which the adhesion of copper conductors (12, 22) to a low-dielectric constant insulating layer (10, 16) is improved. During the fabrication of the structure, exposed surfaces of the low-k insulating layers (10, 16), including the surfaces of these layers within contact, via, or trench openings, are exposed to nitrogen gas, preferably in a sputtering chamber. An optional plasma treatment of the insulating layers (10, 16) in the presence of nitrogen gas may also be performed. As a result, the surface portions of the insulating layers (10, 16) is made to be nitrogen-rich. A liner layer (8, 21) is then formed by reactive sputtering of tantalum nitride over the nitrogen-rich surfaces of the insulating layers (10, 16), followed by the sputtering of tantalum. Copper electrodes (12, 22) are then deposited into the openings in the corresponding insulating layers (10, 16) with improved adhesion resulting.

> (15) Other methods of improving the adhesion of a TaN/Ta bilayer liner to a low-k dielectric have been considered. One such approach is the deposition of a silicon dioxide cap over the low-k dielectric, to which the TaN/Ta bilayer liner adheres relatively well. While this approach may improve adhesion at the top surface of the dielectric, no oxide cap on can be formed the sidewalls of vias or trenches etched through the dielectric layer, so that the adhesion of the copper system will still be weak at those locations. The oxide cap cannot be formed after via or trench etch, of course, without severely limiting the size of the via or trench. Cleanup approaches, such as a hydrogen/helium reactive sputtering etch clean, may or may not improve adhesion, but will definitely require new hardware and an additional chamber.

> 22) Following process 32, or process 34 if performed, process 36 is next carried out to reactively sputter tantalum nitride over the treated surface of low-k dielectric layers 16, 10, and into the via in contact with first level copper conductor 12. Process 36 is performed by energizing the plasma (if not already energized in process 34), and biasing the wafer and tantalum target, in the presence of the nitrogen and argon sputtering gases. Under these conditions, tantalum atoms are sputtered into the chamber, with at least a large portion of these atoms reacting with nitrogen to form tantalum nitride, which then deposits onto the surface of the wafer. It is also contemplated that some of the sputtered tantalum atoms react with the nitrogen in the nitrogen-rich surface portions of the low-k dielectric layers 16, 10, and that this reaction mechanism provides a resulting tantalum nitride layer in the liner layer 21 that is extremely well adhered to low-k dielectric layers 16, 10.

Therefore, it would have been obvious to one of ordinary skill in the art to use Wu's tantalum layer and tantalum rich nitride layer to modify Lopatin's HTS layer for the purpose of achieving excellent adhesion.

Claims 4 and 5 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Hartner et al. (U.S. Patent # 6,649,483 B2) in view of Wo (U.S. Patent # 6,667,231 B1).

Hartner et al. show the features of the claimed invention as detailed above, but fail to explicitly show a layer of tantalum layer over the HTS layer or wherein the barrier layer comprises a layer of a tantalum-rich nitride over the HTS layer, and further comprising a layer of tantalum.

Wu et al. is cited for showing barrier films for copper metallizations over low dielectric contant insulators in a integrated circuit. Specifically, Wu (figures 1a to 2i) specifically figure 1a discloses a layer of tantalum layer (see column 3, lines 25-37) or wherein the barrier layer comprises a layer of a tantalum-rich nitride for the excellent adhesion.

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US-PAT-NO:             6667231

DOCUMENT-IDENTIFIER:   US 6667231 B1

TITLE:                 Method of forming barrier films for
copper metallization
                      over low dielectric constant insulators in
an integrated
                      circuit

DATE-ISSUED:           December 23, 2003

INVENTOR-INFORMATION:
NAME                           CITY                      STATE
ZIP CODE  COUNTRY
Wu; Lixin                      Plano                     TX
N/A       N/A

ASSIGNEE INFORMATION:
NAME                     CITY                      STATE     ZIP
CODE  COUNTRY   TYPE CODE
Texas Instruments        Dallas                    TX        N/A
N/A       02
Incorporated

APPL-NO:       10/ 195006

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ABSTRACT:

An integrated circuit structure and method of making the same is disclosed, in which the adhesion of copper conductors (12, 22) to a low-dielectric constant insulating layer (10, 16) is improved. During the fabrication of the structure, exposed surfaces of the low-k insulating layers (10, 16), including the surfaces of these layers within contact, via, or trench openings, are exposed to nitrogen gas, preferably in a sputtering chamber. An optional plasma treatment of the insulating layers (10, 16) in the presence of nitrogen gas may also be performed. As a result, the surface portions of the insulating layers (10, 16) is made to be nitrogen-rich. A liner layer (8, 21) is then formed by reactive sputtering of tantalum nitride over the nitrogen-rich surfaces of the insulating layers (10, 16), followed by the sputtering of tantalum. Copper electrodes (12, 22) are then deposited into the openings in the corresponding insulating layers (10, 16) with improved adhesion resulting.

(15) Other methods of improving the adhesion of a TaN/Ta bilayer liner to a low-k dielectric have been considered. One such approach is the deposition of a silicon dioxide cap over the low-k dielectric, to which the TaN/Ta bilayer liner adheres relatively well. While this approach may improve adhesion at the top surface of the dielectric, no oxide cap on can be formed the sidewalls of vias or trenches etched through the dielectric layer, so that the adhesion of the copper system will still be weak at those locations. The oxide cap cannot be formed after via or trench etch, of course, without severely limiting the size of the via or trench. Cleanup approaches, such as a hydrogen/helium reactive sputtering etch clean, may or may not improve adhesion, but will definitely require new hardware and an additional chamber.

> 22) Following process 32, or process 34 if performed, process 36 is next carried out to reactively sputter tantalum nitride over the treated surface of low-k dielectric layers 16, 10, and into the via in contact with first level copper conductor 12. Process 36 is performed by energizing the plasma (if not already energized in process 34), and biasing the wafer and tantalum target, in the presence of the nitrogen and argon sputtering gases. Under these conditions, tantalum atoms are sputtered into the chamber, with at least a large portion of these atoms reacting with nitrogen to form tantalum nitride, which then deposits onto the surface of the wafer. It is also contemplated that some of the sputtered tantalum atoms react with the nitrogen in the nitrogen-rich surface portions of the low-k dielectric layers 16, 10, and that this reaction mechanism provides a resulting tantalum nitride layer in the liner layer 21 that is extremely well adhered to low-k dielectric layers 16, 10.

Therefore, it would have been obvious to one of ordinary skill in the art to use Wu's tantalum layer and tantalum rich nitride layer to modify Hartner et al.'s HTS layer for the purpose of achieving excellent adhesion.

The listed references are cited as of interest to this application, but not applied at it time.

Field of Search	Date
U.S. Class and subclass: 257/700,701,758,759,760,764,762,766,298,664,663,665,751	8/8/05
Other Documentation: foreign patents and literature in 257/700,701,758,759,760,764,762,766,298,664,663,665,751	8/8/05
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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Alexander O Williams
Primary Examiner
Art Unit 2826

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